ML4062-SLB V4.0

MSA Compliant 50G (rev2.8)

QSFP-DD Electrical Passive Loopback Module

Rev 0.32

Innovation for the next generation

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ML4062-SLB QSFP-DD 4x28G Passive Loopback Modules – Key Features

- ✓ Supports 8x50G electrical interface
- ✓ QSFP-DD MSA Form Factor
- ✓ Microcontroller can be programmed to maintain user specified PD or constant temperature
- ✓ Built with advanced PCB material
- ✓ 4 Thermistors on PCBA
- ✓ 4 independent power heathers, with 0.1W resolution, up to 14W
- ✓ Temperature Monitor and alarms warning
- ✓ Superior SI performance
- ✓ MSA Compatible Configuration and EEPROM
- ✓ Loops back TX to RX on all 8 ports
- ✓ I2C Interface
- ✓ Programmable MSA memory pages
- ✓ I2C control from edge connectors and from rear pin header
- ✓ 2 status LED Indicator
- ✓ Insertions counter
- ✓ Hot Pluggable module
- ✓ Cut-off temperature preventing module overheating
- ✓ Controller card with I2C Master, supports multiple modules, USB master
- ✓ Cable assemblies for power & I2C Control
- ✓ Custom memory maps
- ✓ Confirm CDAUI-8 compliance for 56G PAM-4

LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.

Red (Solid) – Signifies the module is operating in low power mode.

Green / Red – Signifies that an alarm is asserted.

Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		0		90	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.5	V
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		14	W
Bit Rate		28G NRZ 56G PAM4			56.25	Gbps

1. General Description

QSFP-DD Passive Loopback Module, **ML4062-SLB**, is used for testing QSFP-DD transceiver ports under board level tests. By substituting a full-featured QSFP-DD transceiver with the ML4062-SLB, its electrical loopback provides a cost effective low loss method for QSFP-DD port testing.

The **ML4062-SLB** is packaged in a standard MSA housing compatible with all QSFP-DD ports. Transmit data from the host is electrically routed, (internal to the loopback module), to the receive data outputs and back to the host. It provides an economical way to exercise QSFP-DD ports during R&D validation, production testing, and field testing.

2. Functional Description

2.1 Management Data Interface – I2C

The ML4062 supports the I2C interface. This QSFP-DD datasheet is based on the QSFP-DD specification Rev2.8.

2.2 I2C Signals, Addressing and Frame Structure

2.2.1 QSFP-DD Timing Diagram

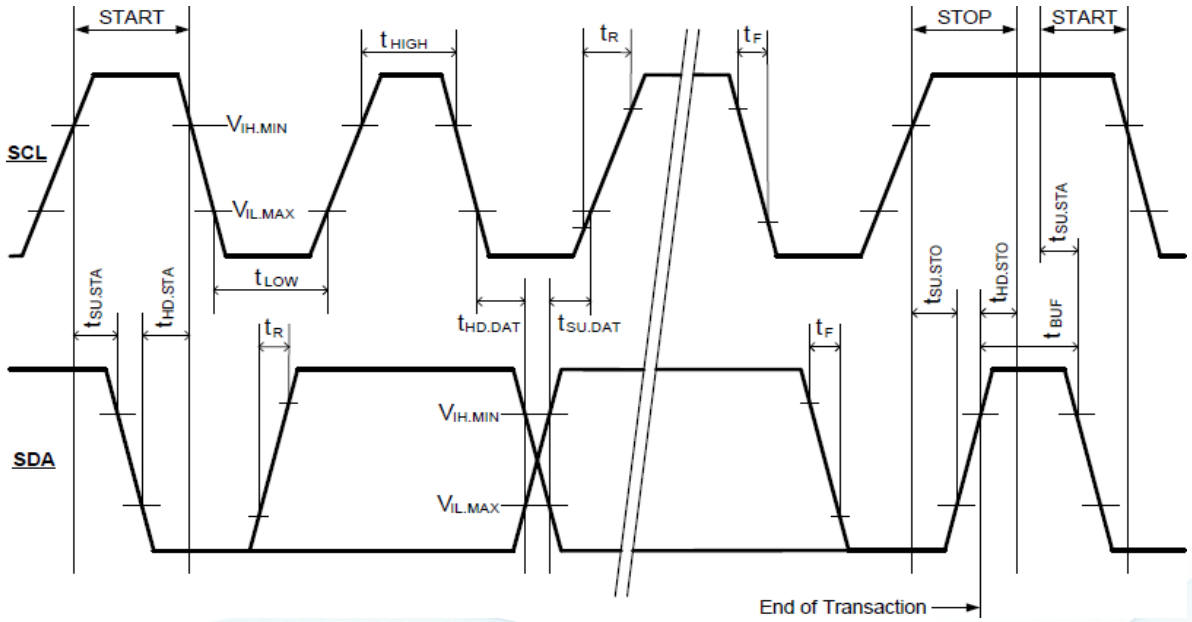


Figure 1: QSFP-DD Timing Diagram

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied.

2.2.2 Management Interface Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in the table below.

		Fast Mode (400 KHz)		
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	fSCL	0	1	MHz
Clock Pulse Width Low	tLOW	1.3		us
Clock Pulse Width High	tHigh	0.6		us
Time bus free before new transmission can start	tBUF	20		us
START Hold Time	tHD.STA	0.6		us
START Set-up Time	tSU.STA	0.6		us
Data In Hold Time	tHD.DAT	0		us
Data in Setup Time	tSU.DAT	0.1		us
Input Rise Time (400kHz)	tR.400		300	ns
Input Fall Time (400kHz)	tF.400		300	ns
STOP Setup Time	tSU.STO	0.6		us
ModSelL Setup Time	tSU.ModSelL	2		ms
ModSelL Hold Time	tHD.ModSelL	2		ms
Aborted sequence – bus release	Deselect_Abort	2		ms

2.2.3 Memory Specifications

QSFP-DD memory transaction timings are given in the following table:

Parameter	Symbol	Min	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us
Complete Single or Sequential Write	tWR		40	ms
Endurance (Write Cycles)		50K		cycles

2.3 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModSelL
- ResetL
- InitMode
- ModPrsL
- IntL

2.3.1 ModSelL

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

2.3.2 ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

2.3.3 InitMode

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

2.3.4 ModPrsL

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

2.3.5 IntL

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

2.4 QSFP-DD Memory Map

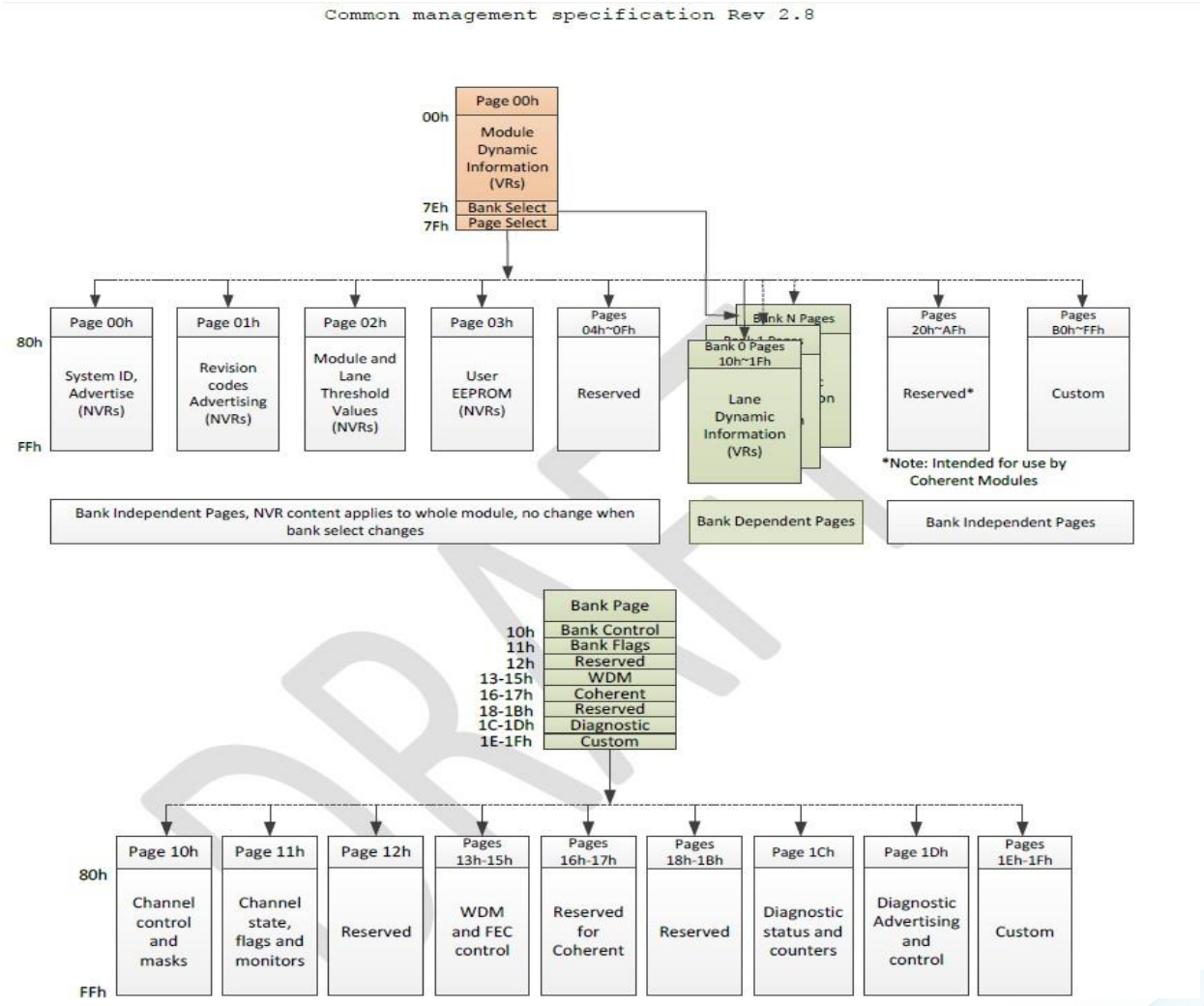


Figure 2: QSFP-DD Memory Map

This section defines the Memory Map for QSFP-DD Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices.

The structure of the memory is shown in Figure 2. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides a user read/write space. The lower page and upper page 00 are always implemented. Page 03 is required if byte 2, bit 2 in the lower page is low.

2.5 ML4062-SLB Specific Functions

2.5.1 Module State

The Module State describes module-wide behaviors and properties. The ML4062-SLB implements two module states: ModuleReady and ModuleLowPwr.

The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the device is in Low Power mode, the Led turns into Red and the PWM is deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.

The ModuleReady state is a host control state that indicates that the module is in High Power mode, the Led turns into Green and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module	RO

2.5.2 Module State Transition

The module only observes the state of the InitMode signal during the MgmtInit state (after module plug-in or Reset), to determine the Init mode, that could be one of two possibilities: Hardware or Software Init mode. Any host changes to the InitMode signal that occur after MgmtInit will not be applied until the module is reset or power cycled.

If InitMode =1, module is booting in Software Init mode, where module is in Low Power mode. In this case, transition to High Power mode is done by:

1. Writing to register 128 Page 16 any value other than 0
2. register 26 bit 4 should be 0 (ForceLowPower = 0)

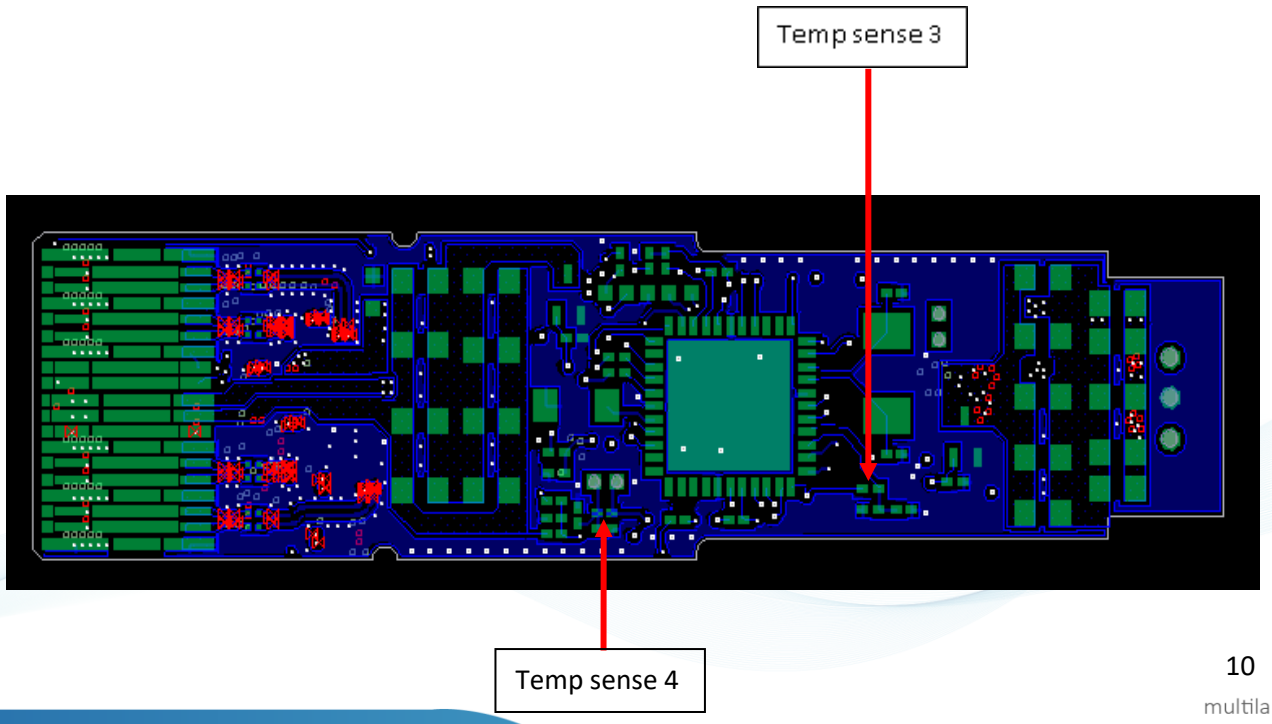
Then the Module State Machines shall transition to ModuleReady (module is in High Power mode).

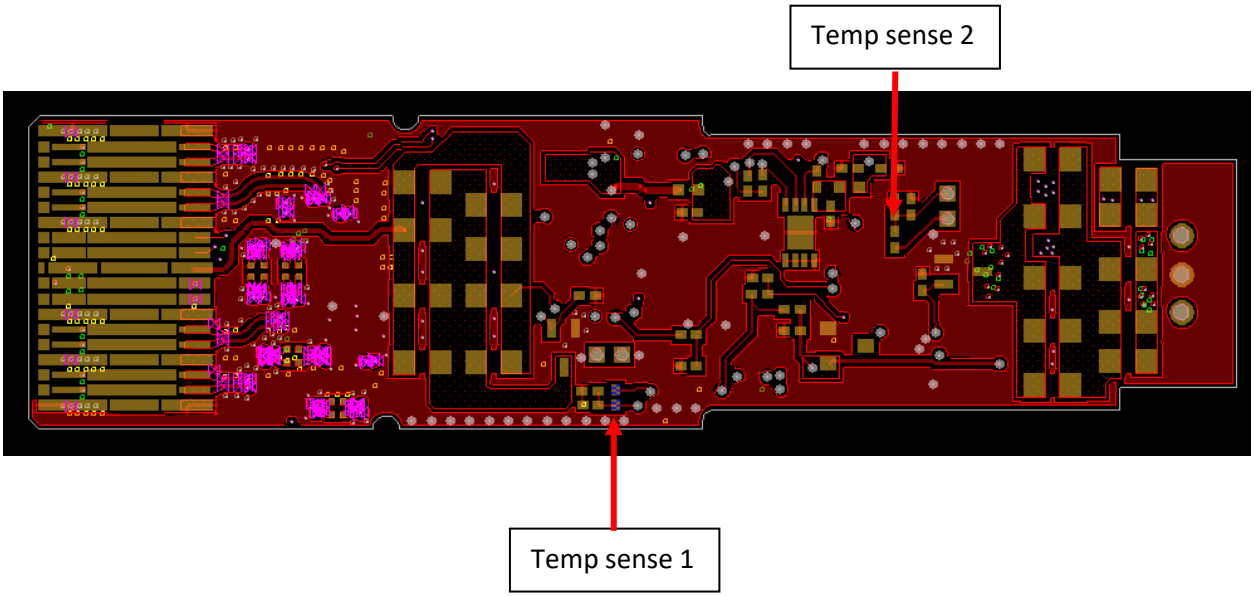
Return to Low Power mode is allowed by writing 1 to register 26 bit 4 (ForceLowPower = 1) – refer to section 2.5.9.

If InitMode = 0, module is booting in Hardware Init mode, where module is in High Power mode. To return to Low Power mode user should write 1 to register 26 bit 4 (ForceLowPower = 1), where the Module State Machines shall transition to ModuleLowPwr.

2.5.3 Temperature Monitor

The ML4062-SLB has 4 internal temperature sensors in order to continuously monitor the module's temperature. The temperature sensor readings are present in low-memory registers. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –128C to +128C that is considered valid between –40 and +125C. Temperature accuracy is less than 1 degree Celsius over specified operating temperature and voltage. Please check below for details on the location of temperature sensors.





Address	Bit	Name	Description
14 (lower Page)	ALL	Temperature MSB	Internally measured module temperature 3
15 (lower Page)	ALL	Temperature LSB	Internally measured module temperature 3
24 (lower Page)	ALL	Custom Temperature MSB	Internally measured module temperature 1
25 (lower Page)	ALL	Custom Temperature LSB	Internally measured module temperature 1
152 Page 3	ALL	Temperature MSB	Internally measured module temperature 2
153 Page 3	ALL	Temperature LSB	Internally measured module temperature 2
154 page 3	ALL	Temperature MSB	Internally measured module temperature 4
155 page 3	ALL	Temperature LSB	Internally measured module temperature 4

The temperature Alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag
	2	L-Temp High Warning	Latched high temperature warning flag
	1	L-Temp Low Alarm	Latched low temperature alarm flag
	0	L-Temp High Alarm	Latched high temperature alarm flag

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

2.5.4 Voltage Sense

A voltage sense circuit is available in the ML4062-SLB that allows to measure the internal module supplied voltage Vcc. Supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) with LSB equal to 100 uVolt, yielding a total measurement range of 0 to +6.55 Volts.

Address	Bit	Name	Description
16 (lower Page)	ALL	Supply Voltage MSB	Internally measured module Supply Voltage
17 (lower Page)	ALL	Supply Voltage LSB	Internally measured module Supply Voltage

The Voltage Alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description
9 (lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag

2.5.5 Thermal Loads Mode Select

The thermal loads can be programmed in two modes.

Register 129 of memory page 3 allows to switch between the two modes.

Address	Bit	Name	Description
129 (Page 03)	0	Thermal Loads Mode Select	0: user specified power dissipation (default) 1: maintain constant temperature

1. Constant Power

Registers 135 to 138 of page 3 are used for PWM control over I2C. These are 8 bit data wide register.

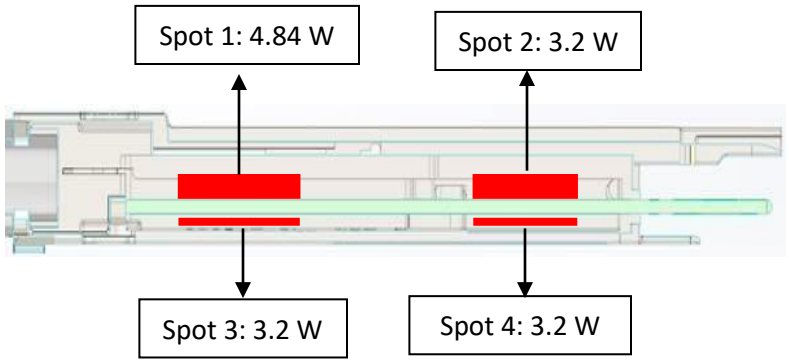
The consumed power changes accordingly when the value in this register is changed (only when in high power mode). The values written in this register are permanently stored.

The PWM can also be used for module thermal emulation.

The module contains 4 thermal spots positioned where the optical transceivers usually are in an optical module that is heated relative to the related PWM register. One spot is 4.84 W and three are 3.2 W. The power can be configured with a 0.1 W resolution.

Address	Bit	Name	Description
135 Page 03	7:0	4.84 W power controller 1	4.48 W top power spot control register, powered by P3V3 net
136 Page 03	7:0	3.2 W power controller 2	3.2 W top power spot control register, powered by P3V3_Vcc1 net
137 Page 03	7:0	3.2 W PWM controller 3	3.2 W bottom power spot PWM control register, powered by P3V3_VccTx net
138 Page 03	7:0	3.2 W PWM controller 4	3.2 W bottom power spot PWM control register, powered by P3V3_VccRx net

In the figure below, the red spots represents the 4 thermal spots on the module.



2. Constant Temperature

The module can be programmed to maintain a constant temperature. Register 130 of memory page 3 is used to set the desired temperature. This temperature follows the temperature in register 14 and 15.

Address	Bit	Name	Description
130 (Page 03)	7:0	Target temperature	Target Temperature to be maintained by the module, LSB = 1 degC

2.5.6 Status registers

Register 139 of page 3 reports the digital state of the QSFP-DD low speed signals and controls IntL pin.

Address	Bit	Name	Description
139 (Page 03)	0	ModSel	Digital state of ModSel pin
	1	InitMode	Digital state of InitMode

Note that when the ModSelL is High the I2C will stop working and the user will read FF from register 139.

2.5.7 Digital state detection

The module must able to detect the digital state of the InitMode and ModSelL signals. An I2C latch register in upper page 03 should be latched on both rising and falling edges of the InitMode and ModSelL signals.

Address	Bit	Name	Description
139 (Page 03)	4	ModSelL transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register
	5	InitMode transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register

2.5.8 Digital Control of IntL

During power-up of the module, IntL is defaulted to negated. Afterward, host can set the status of this signal to any status through an I2C register in upper page 03.

Address	Bit	Name	Description
140 (Page 03)	1 0	IntL control	0xb: Normal operation 10b: Force IntL to logic 0, VIntL < Vol(max) 11b: Force IntL to logic 1, VIntL > Voh(min)

2.5.9 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
26(lower Page)	4	ForceLowPwr	0b= high power mode(default) 1b=Forces module into low power mode	RW
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=not in reset 1b=Software reset	

Address	Bit	Name	Description	Type
3 (lower Page)	0	Interrupt	Digital state of Interrupt output signal 0b=Interrupt asserted 1b=Interrupt not asserted (default)	RO

2.5.10 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from registers 132 and 133 of memory page 3.

Address	Bit	Name	Description
132(Page 03)	ALL	Insertion Counter MSB	LSB unit = 1 insertion
133(Page 03)	ALL	Insertion Counter LSB	

2.5.11 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.

The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.

The Cut-Off temperature for the ML4062-SLB is 85°C and it can be programmed to any value from register 134 of memory page 3.

Address	Bit	Name	Description	Type
134(Page 03)	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW

2.5.12 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is outside of "normal" limits. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128(Page 02)	ALL	high temp alarm threshold (MSB)	80˚C	RW
129(Page 02)	ALL	high temp alarm threshold (LSB)		
130(Page 02)	ALL	low temp alarm threshold (MSB)	0˚C	
131(Page 02)	ALL	low temp alarm threshold (LSB)		
132(Page 02)	ALL	high temp warning threshold (MSB)	75˚C	
133(Page 02)	ALL	high temp warning threshold (LSB)		
134(Page 02)	ALL	low temp warning threshold (MSB)	5˚C	
135(Page 02)	ALL	low temp warning threshold (LSB)		
136(Page 02)	ALL	high volt alarm threshold (MSB)	3.6 V	
137(Page 02)	ALL	high volt alarm threshold (LSB)		
138(Page 2)	ALL	low volt alarm threshold (MSB)	3.0 V	
139(Page 2)	ALL	low volt alarm threshold (LSB)		
140(Page 2)	ALL	high volt warning threshold (MSB)	3.55 V	
141(Page 2)	ALL	high volt warning threshold (LSB)		
142(Page 2)	ALL	low volt warning threshold (MSB)	3.05 V	
143(Page 2)	ALL	low volt warning threshold (LSB)		

3. QSFP-DD Pin Allocation

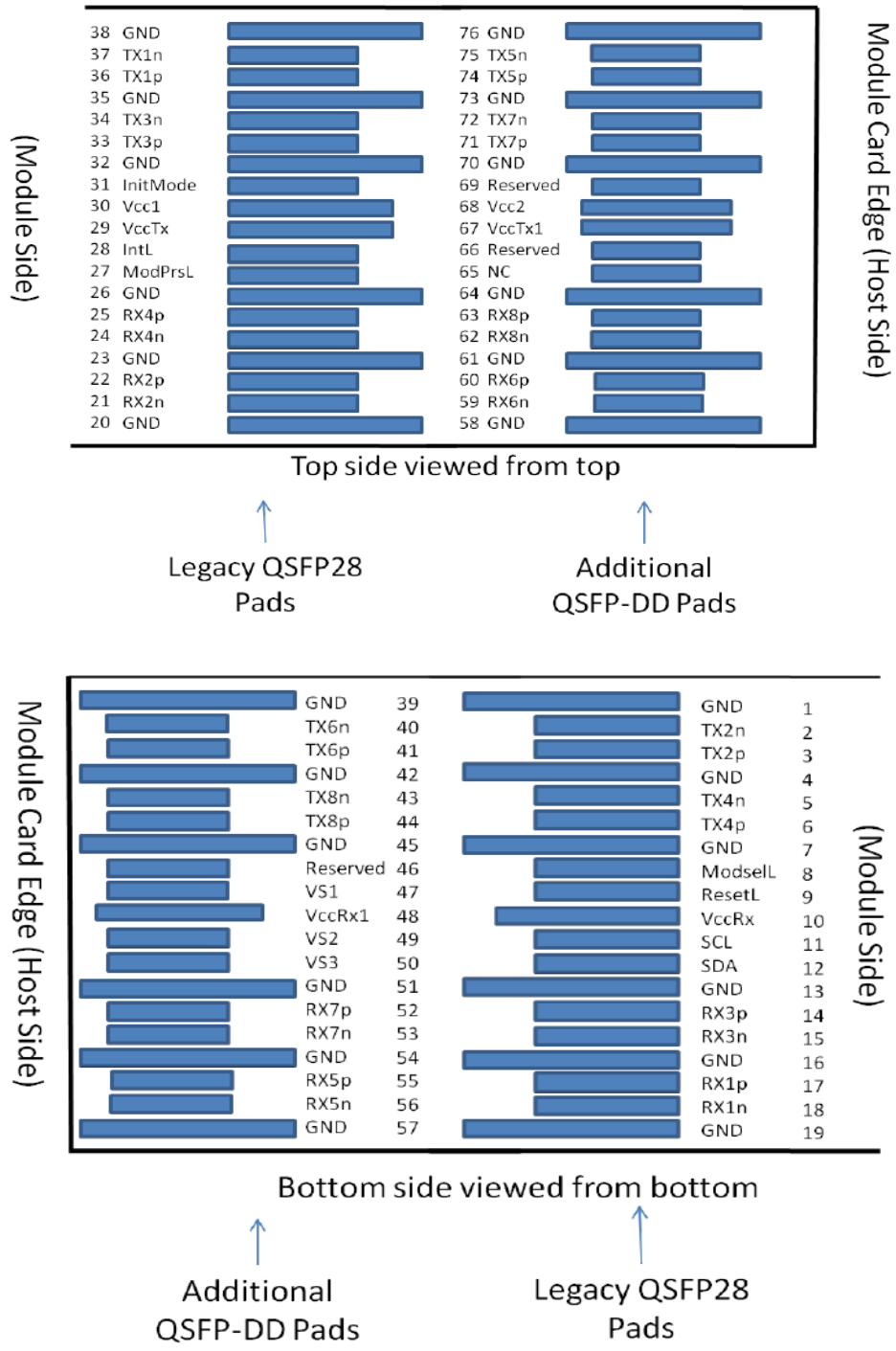


Figure 3: QSFP-DD Module Pad Layout

Revision History

Revision number	Date	Description
0.1	14/06/2018	▪ Preliminary
0.2	9/07/2018	▪ Update section 2.5.11
0.3	5/4/2019	▪ add section: Module State Transition (2.5.2)

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